ABSTRACT

A method and processor for multiplication operation instruction processing are provided. Multiplication operation instructions are executed on source operands in data memory locations. The multiplication operation instructions are provided to perform complex multiplication operations. The multiplication operation instructions may generate the square of a multiplication source operand and generate the difference of a subtrahend source operand and a minuend source operand simultaneously. The square is output to a target accumulator specified in the multiplication operation instruction. The difference is output to a difference register specified in the multiplication operation instruction. In the alternative, the multiplication operation instructions may generate the sum of the square of multiplication source operand and an addition operand as well as generate the difference of a subtrahend source operand and a minuend source operand simultaneously. The sum is output to a target accumulator specified in the multiplication operation instruction. The difference is output to a difference register specified in the multiplication operation instruction.